1. GENERAL DESCRIPTION

EM78156E is an 8-bit microprocessor with low-power and high-speed CMOS technology. Integrated into a single chip are on-chip watchdog timer (WDT), RAM, ROM, real time clock/counter, external and interrupt, power down mode, and tri-state I/O.

2. FEATURES

- Operating voltage range : 2.3V~5.5V
- Operating temperature range: 0°C~70°C
- Operating frequency rang (base on 2 clocks):
  * Crystal mode: DC~20MHz at 5V, DC~8MHz at 3V, DC~4MHz at 2.3V.
  * ERC mode: DC~4MHz at 5V, DC~4MHz at 3V, DC~4MHz at 2.3V.
- Low power consumption:
  * Less then 1.6 mA at 5V/4MHz
  * Typically 15 μA at 3V/32KHz
  * Typically 1 μA during sleep mode
- 1K × 13 bits on chip ROM
- One configuration register to accommodate user's requirements
- 48× 8 bits on chip registers (SRAM, general purpose register)
- 2 bi-directional I/O ports
- 5 level stacks for subroutine nesting
- 8-bit real time clock/counter (TCC) with selective signal sources, trigger edges, and overflow interrupt
- Two clocks per instruction cycle
- Power down (SLEEP) mode
- Three available interruptions
  * TCC overflow interrupt
  * Input-port status changed interrupt (wake up from sleep mode)
  * External interrupt
- Programmable free running watchdog timer
- 8 programmable pull-high pins
- 7 programmable pull-down pins
- 8 programmable open-drain pins
- 2 programmable R-option pins
- Package types:
  * 18 pin DIP 300mil : EM78156EP
  * 18 pin SOP(SOIC) 300mil : EM78156EM
  * 20 pin SSOP 209mil : EM78156EAS

* 20 pin SSOP 209mil : EM78P156EKM

• 99.9% single instruction cycle commands

• The transient point of system frequency between HXT and LXT is around 400KHz

3. PIN ASSIGNMENT

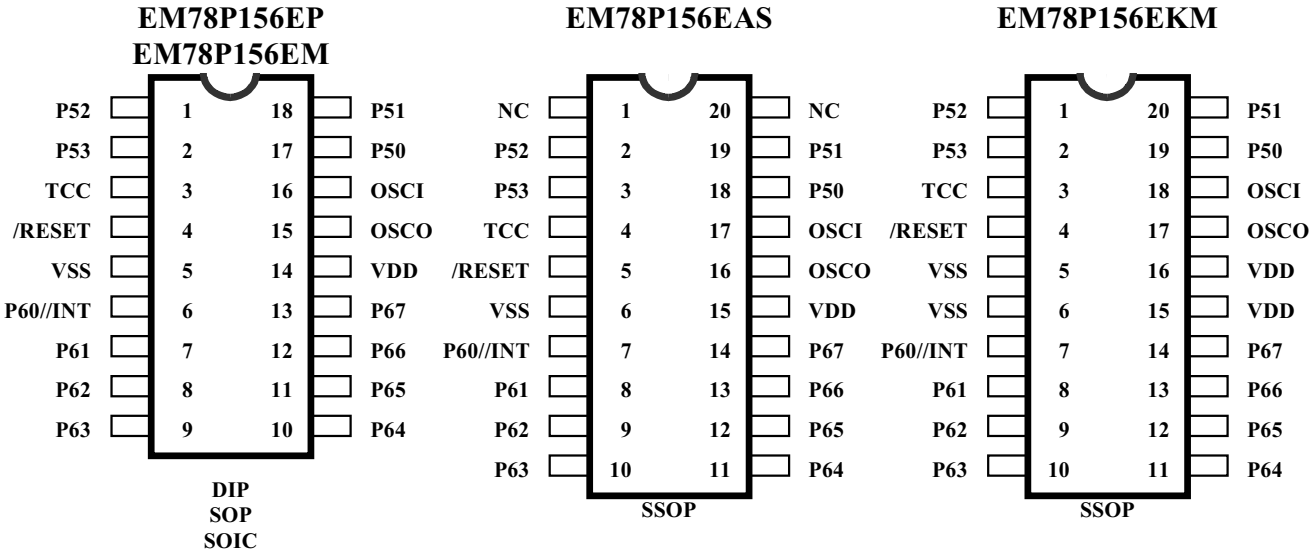


Fig. 1 Pin Assignment

Table 1 EM78156EP and EM78156EM Pin Description

Symbol	Pin No.	Type	Function
VDD	14	-	* Power supply.
OSCI	16	I	* XTAL type: Crystal input terminal or external clock input pin. * ERC type: RC oscillator input pin.
OSCO	15	I/O	* XTAL type: Output terminal for crystal oscillator or external clock input pin. * RC type: Instruction clock output. * External clock signal input.
TCC	3	I	* The real time clock/counter (with Schmitt trigger input pin), must be tied to VDD or VSS if not in use.
/RESET	4	I	* Input pin with Schmitt trigger. If this pin remains at logic low, the controller will also remain in reset condition.
P50~P53	17, 18, 1, 2	I/O	*P50~P53 are bi-directional I/O pins. *P50 and P51 can also be defined as the R-option pins. *P50~P52 can be pulled-down by software.
P60~P67	6~13	I/O	* P60~P67 are bi-directional I/O pins. * These can be pulled-high or can be open-drain by software programming. * P60~P63 can also be pulled-down by software.
/INT	6	I	* External interrupt pin triggered by falling edge.
VSS	5	-	* Ground.

Table 2 EM78156EAS Pin Description

Symbol	Pin No.	Type	Function
VDD	15	-	* Power supply.
OSCI	17	I	* XTAL type: Crystal input terminal or external clock input pin. * ERC type: RC oscillator input pin.
OSCO	16	I/O	* XTAL type: Output terminal for crystal oscillator or external clock input pin. * RC type: Instruction clock output. * External clock signal input.
TCC	4	I	* The real time clock/counter (with Schmitt trigger input pin), must be tied to VDD or VSS if not in use.
/RESET	5	I	* Input pin with Schmitt trigger. If this pin remains at logic low, the controller will also remain keep in reset condition.
P50~P53	18, 19, 2, 3	I/O	* P50~P53 are bi-directional I/O pins. * P50 and P51 can also be defined as the R-option pins. * P50~P52 can also be pulled-down by software.
P60~P67	7~14	I/O	* P60~P67 are bi-directional I/O pins. * These can be pulled-high or can be open-drain by software programming. * P60~P63 can be pulled-down also by software.
/INT	7	I	* External interrupt pin triggered by falling edge.
VSS	6	-	* Ground.

Table 3 EM78P156EKM Pin Description

Symbol	Pin No.	Type	Function
VDD	15,16	-	* Power supply.
OSCI	18	I	* XTAL type: Crystal input terminal or external clock input pin. * ERC type: RC oscillator input pin.
OSCO	17	I/O	* XTAL type: Output terminal for crystal oscillator or external clock input pin. * RC type: Instruction clock output. * External clock signal input.
TCC	3	I	* The real time clock/counter (with Schmitt trigger input pin), must be tied to VDD or VSS if not in use.
/RESET	4	I	* Input pin with Schmitt trigger. If this pin remains at logic low, the controller will also remain in reset condition.
P50~P53	19, 20, 1, 2	I/O	* P50~P53 are bi-directional I/O pins. * P50 and P51 can also be defined as the R-option pins. * P50~P52 can be pulled-down by software.
P60~P67	7~14	I/O	* P60~P67 are bi-directional I/O pins. * These can be pulled-high or can be open-drain by software programming. * P60~P63 can also be pulled-down by software.
/INT	7	I	* External interrupt pin triggered by falling edge.
VSS	5, 6	-	* Ground.

4. FUNCTION DESCRIPTION

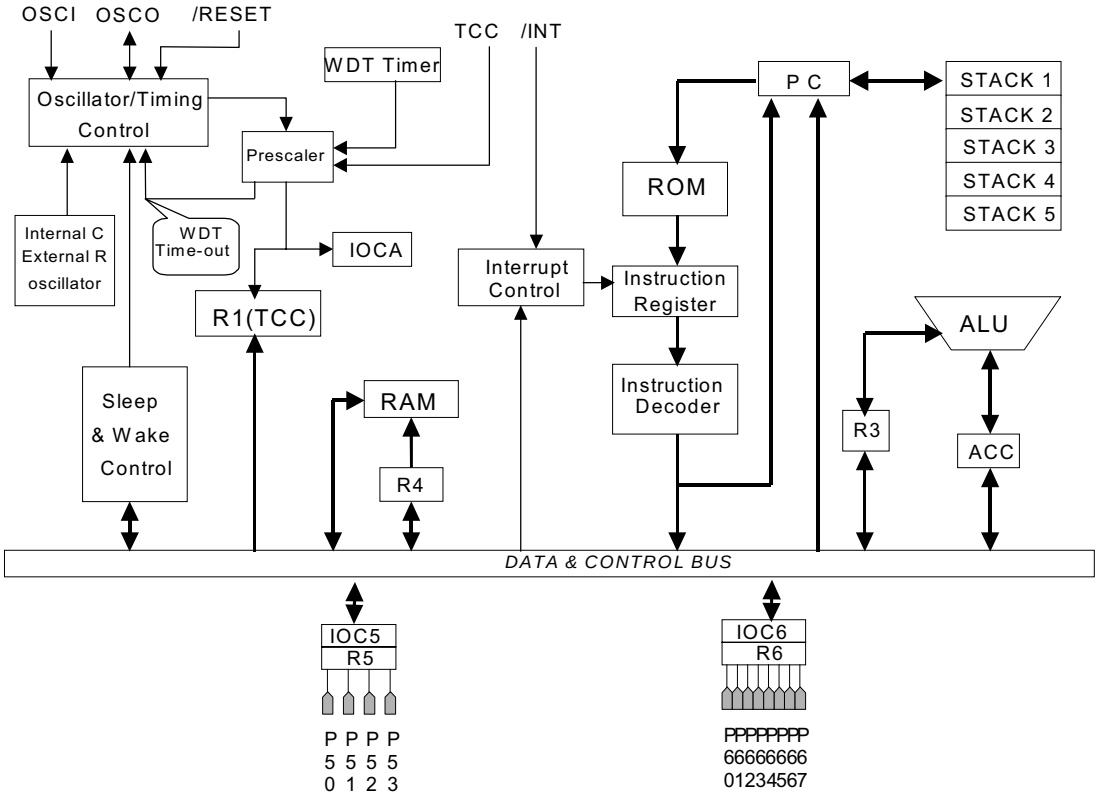


Fig. 2 Function Block Diagram

4.1 Operational Registers

1. R0 (Indirect Addressing Register)

R0 is not a physically implemented register. Its major function is to perform as an indirect addressing pointer. Any instruction using R0 as a pointer actually accesses data pointed by the RAM Select Register (R4).

2. R1 (Time Clock /Counter)

- Increased by an external signal edge which is defined by TE bit (CONT-4) through the TCC pin, or by the instruction cycle clock.
- Writable and readable as any other registers.

• Defined by resetting PAB(CONT-3).

• The prescaler is assigned to TCC, if the PAB bit (CONT-3) is reset.

• The contents of the prescaler counter will be cleared only when TCC register is written with a value.

3. R2 (Program Counter) & Stack

• Depending on the device type, R2 and hardware stack are 10-bit wide. The structure is depicted in Fig.3.

• Generating 1024×13 bits on-chip ROM addresses to the relative programming instruction codes. One program page is 1024 words long.

• R2 is set as all "0"s when under RESET condition.

• "JMP" instruction allows direct loading of the lower 10 program counter bits. Thus, "JMP" allows PC to go to any location within a page.

• "CALL" instruction loads the lower 10 bits of the PC, and then PC+1 is pushed into the stack. Thus, the subroutine entry address can be located anywhere within a page.

• "RET" ("RETL k", "RETI") instruction loads the program counter with the contents of the top-level stack.

• "ADD R2,A" allows the contents of 'A' to be added to the current PC, and the ninth and tenth bits of the PC are cleared.

• "MOV R2,A" allows to load an address from the "A" register to the lower 8 bits of the PC, and the ninth and tenth bits of the PC are cleared.

• Any instruction that writes to R2 (e.g. "ADD R2,A", "MOV R2,A", "BC R2,6",·····) will cause the ninth and tenth bits (A8~A9) of the PC to be cleared. Thus, the computed jump is limited to the first 256 locations of a page.

• All instruction are single instruction cycle (fclk/2 or fclk/4) except for the instruction that would change the contents of R2. Such instruction will need one more instruction cycle.

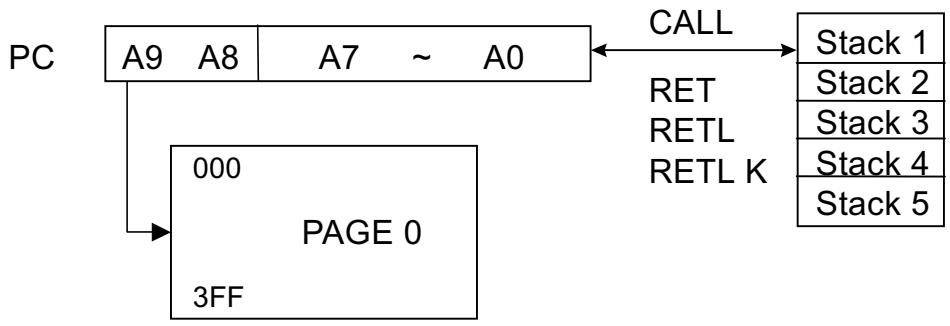


Fig. 3 Program Counter Organization

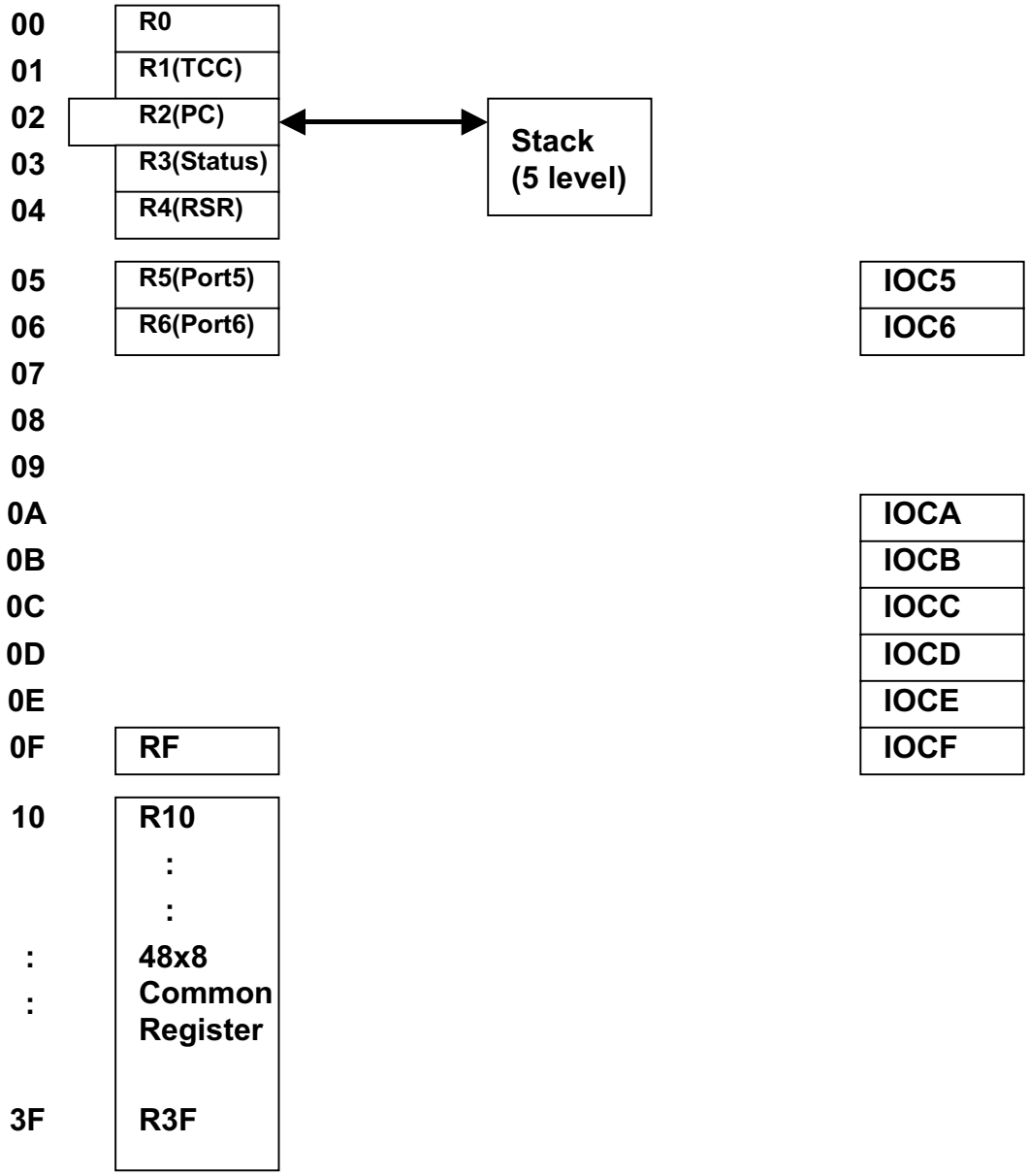


Fig. 4 Data Memory Configuration

4. R3 (Status Register)

7	6	5	4	3	2	1	0
GP2	GP1	GP0	T	P	Z	DC	C

- **Bit 0 (C)** Carry flag
- **Bit 1 (DC)** Auxiliary carry flag
- **Bit 2 (Z)** Zero flag.

  Set to "1" if the result of an arithmetic or logic operation is zero.
- **Bit 3 (P)** Power down bit.

Set to 1 during power on or by a "WDTC" command and reset to 0 by a "SLEP" command.

• **Bit 4 (T)** Time-out bit.

Set to 1 with the "SLEP" and "WDTC" commands, or during power up and reset to 0 by WDT time-out.

• **Bit5 ~7 (GP0 ~ 2)** General purpose read/write bits.

5. R4 (RAM Select Register)

• Bits 0~5 are used to select registers (address: 00~06, 0F~3F) in the indirect addressing mode.

• Bits 6~7 are not used.(read only).

• The Bits 6~7 set to “1” at all time.

•Z flag of R3 will set to “1”, when R4 content is equal to “3F” When R4=R4+1, R4 content will select as R0.

• See the configuration of the data memory in Fig. 4.

6. R5 ~ R6 (Port 5 ~ Port 6)

• R5 and R6 are I/O registers.

• Only the lower 4 bits of R5 are available.

7. RF (Interrupt Status Register)

7	6	5	4	3	2	1	0
-	-	-	-	-	EXIF	ICIF	TCIF

“1” means interrupt request, and “0” means no interrupt occur.

• **Bit 0 (TCIF)** TCC overflow interrupt flag. Set when TCC overflows, reset by software.

• **Bit 1 (ICIF)** Port 6 input status change interrupt flag. Set when Port 6 input changes, reset by software.

• **Bit 2 (EXIF)** External interrupt flag. Set by falling edge on /INT pin, reset by software.

• **Bits 3 ~ 7** Not used.

• RF can be cleared by instruction but cannot be set.

• IOCF is the interrupt mask register.

• Note that the result of reading RF is the "logic AND" of RF and IOCF.

8. R10 ~ R3F

• All of these are 8-bit general-purpose registers.

4.2 Special Purpose Registers

1. A (Accumulator)

• Internal data transfer, or instruction operand holding

• It cannot be addressed.

2. CONT (Control Register)

7	6	5	4	3	2	1	0
-	/INT	TS	TE	PAB	PSR2	PSR1	PSR0

• Bit 0 (PSR0) ~ Bit 2 (PSR2) TCC/WDT prescaler bits.

PSR2	PSR1	PSR0	TCC Rate	WDT Rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

• **Bit 3 (PAB)** Prescaler assignment bit.

0: TCC

1: WDT

• **Bit 4 (TE)** TCC signal edge

0: increment if the transition from low to high takes place on TCC pin

1: increment if the transition from high to low takes place on TCC pin

• **Bit 5 (TS)** TCC signal source

0: internal instruction cycle clock

1: transition on TCC pin

• **Bit 6 (/INT)** Interrupt enable flag

0: masked by DISI or hardware interrupt

1: enabled by ENI/RETI instructions

• **Bit 7** Not used.

• CONT register is both readable and writable.

3. IOC5 ~ IOC6 (I/O Port Control Register)

• "1" put the relative I/O pin into high impedance, while "0" defines the relative I/O pin as output.

• Only the lower 4 bits of IOC5 can be defined.

• IOC5 and IOC6 registers are both readable and writable.

4. IOCA (Prescaler Counter Register)

• IOCA register is readable.

• The value of IOCA is equal to the contents of Prescaler counter.

• Down counter.

5. IOCB (Pull-down Control Register)

7	6	5	4	3	2	1	0
/PD7	/PD6	/PD5	/PD4	-	/PD2	/PD1	/PD0

- **Bit 0 (/PD0)** Control bit is used to enable the pull-down of P50 pin.

  0: Enable internal pull-down

  1: Disable internal pull-down

- **Bit 1 (/PD1)** Control bit is used to enable the pull-down of P51 pin.
- **Bit 2 (/PD2)** Control bit is used to enable the pull-down of P52 pin.
- Bit 3 Not used.
- **Bit 4 (/PD4)** Control bit is used to enable the pull-down of P60 pin.
- **Bit 5 (/PD5)** Control bit is used to enable the pull-down of P61 pin.
- **Bit 6 (/PD6)** Control bit is used to enable the pull-down of P62 pin.
- **Bit 7 (/PD7)** Control bit is used to enable the pull-down of P63 pin.
- IOCB Register is both readable and writable.

6. IOCC (Open-drain Control Register)

7	6	5	4	3	2	1	0
OD7	OD6	OD5	OD4	OD3	OD2	OD1	OD0

- **Bit 0 (OD0)** Control bit used to enable the open-drain of P60 pin.

  0: Disable open-drain output

  1: Enable open-drain output

- **Bit 1 (OD1)** Control bit is used to enable the open-drain of P61 pin.
- **Bit 2 (OD2)** Control bit is used to enable the open-drain of P62 pin.
- **Bit 3 (OD3)** Control bit is used to enable the open-drain of P63 pin.
- **Bit 4 (OD4)** Control bit is used to enable the open-drain of P64 pin.
- **Bit 5 (OD5)** Control bit is used to enable the open-drain of P65 pin.
- **Bit 6 (OD6)** Control bit is used to enable the open-drain of P66 pin.
- **Bit 7 (OD7)** Control bit is used to enable the open-drain of P67 pin.
- IOCC Register is both readable and writable.

7. IOCD (Pull-high Control Register)

7	6	5	4	3	2	1	0
/PH7	/PH6	/PH5	/PH4	/PH3	/PH2	/PH1	/PH0

- **Bit 0 (/PH0)** Control bit is used to enable the pull-high of P60 pin.

  0: Enable internal pull-high

  1: Disable internal pull-high

• **Bit 1 (/PH1)** Control bit is used to enable the pull-high of P61 pin.

• **Bit 2 (/PH2)** Control bit is used to enable the pull-high of P62 pin.

• **Bit 3 (/PH3)** Control bit is used to enable the pull-high of P63 pin.

• **Bit 4 (/PH4)** Control bit is used to enable the pull-high of P64 pin.

• **Bit 5 (/PH5)** Control bit is used to enable the pull-high of P65 pin.

• **Bit 6 (/PH6)** Control bit is used to enable the pull-high of P66 pin.

• **Bit 7 (/PH7)** Control bit is used to enable the pull-high of P67 pin.

• IOCD Register is both readable and writable.

8. IOCE (WDT Control Register)

7	6	5	4	3	2	1	0
WDTE	EIS	-	ROC	-	-	-	-

• **Bit 7 (WDTE)** Control bit used to enable Watchdog timer.

0: Disable WDT.

1: Enable WDT.

WDTE is both readable and writable.

• **Bit 6 (EIS)** Control bit is used to define the function of P60(/INT) pin.

0: P60, bi-directional I/O pin.

1: /INT, external interrupt pin. In this case, the I/O control bit of P60 (bit 0 of IOC6) must be set to "1".

When EIS is "0", the path of /INT is masked. When EIS is "1", the status of /INT pin can also be read by way of reading Port 6 (R6). Refer to Fig. 7(a).

EIS is both readable and writable.

• **Bit 4 (ROC)** ROC is used for the R-option.

Setting the ROC to "1" will enable the status of R-option pins (P50~P51) that are read by the controller. Clearing the ROC will disable the R-option function. If the R-option function is selected, user must connect the P51 pin or/and P50 pin to VSS with a 430KΩ external resistor (Rex). If the Rex is connected/disconnected, the status of P50 (P51) is read as "0"/"1". Refer to Fig. 8.

• **Bits 0~3,5** Not used.

9. IOCF (Interrupt Mask Register)

7	6	5	4	3	2	1	0
-	-	-	-	-	EXIE	ICIE	TCIE

• **Bit 0 (TCIE)** TCIF interrupt enable bit.

0: disable TCIF interrupt

1: enable TCIF interrupt

- **Bit 1 (ICIE)** ICIF interrupt enable bit.
  0: disable ICIF interrupt
  1: enable ICIF interrupt
- **Bit 2 (EXIE)** EXIF interrupt enable bit.
  0: disable EXIF interrupt
  1: enable EXIF interrupt
- **Bits 3~7** Not used.
- Individual interrupt is enabled by setting its associated control bit in the IOCF to "1".
- Global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. Refer to Fig. 10.
- IOCF register is both readable and writable.

4.3 TCC/WDT & Prescaler

An 8-bit counter available as prescaler for the TCC or WDT. The prescaler is available for either the TCC or WDT only at any given time, and the PAB bit of the CONT register is used to determine the prescaler assignment. The PSR0~PSR2 bits determine the ratio. The prescaler is cleared each time the instruction is written to TCC under TCC mode. The WDT and prescaler, when assigned to WDT mode, are cleared by the “WDTC” or “SLEP” instructions. Fig. 5 depicts the circuit diagram of TCC/WDT.

- R1 (TCC) is an 8-bit timer/counter. The clock source of TCC can be internal or external clock input (edge selectable from TCC pin). If TCC signal source is from internal clock, TCC will increase by 1 at every instruction cycle (without prescaler). Referring to Fig. 5, CLK=Fosc/2 or CLK=Fosc/4 application is determined by the CODE Option bit CLK status. CLK=Fosc/2 is used if CLK bit is "0", and CLK=Fosc/4 is used if CLK bit is "1". If TCC signal source comes from external clock input, TCC is increased by 1 at every falling edge or rising edge of TCC pin.

- The watchdog timer is a free running on-chip RC oscillator. The WDT will keep on running even when the oscillator driver has been turned off (i.e. in sleep mode). During normal operation or sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled any time during normal mode by software programming. Refer to WDTE bit of IOCE register. Without prescaler, the WDT time-out period is approximately 18 ms[1] (default).

[1] <Note>: Vdd = 5V, set up time period = 16.5ms ± 5%
Vdd = 3V, set up time period = 18ms ± 5%

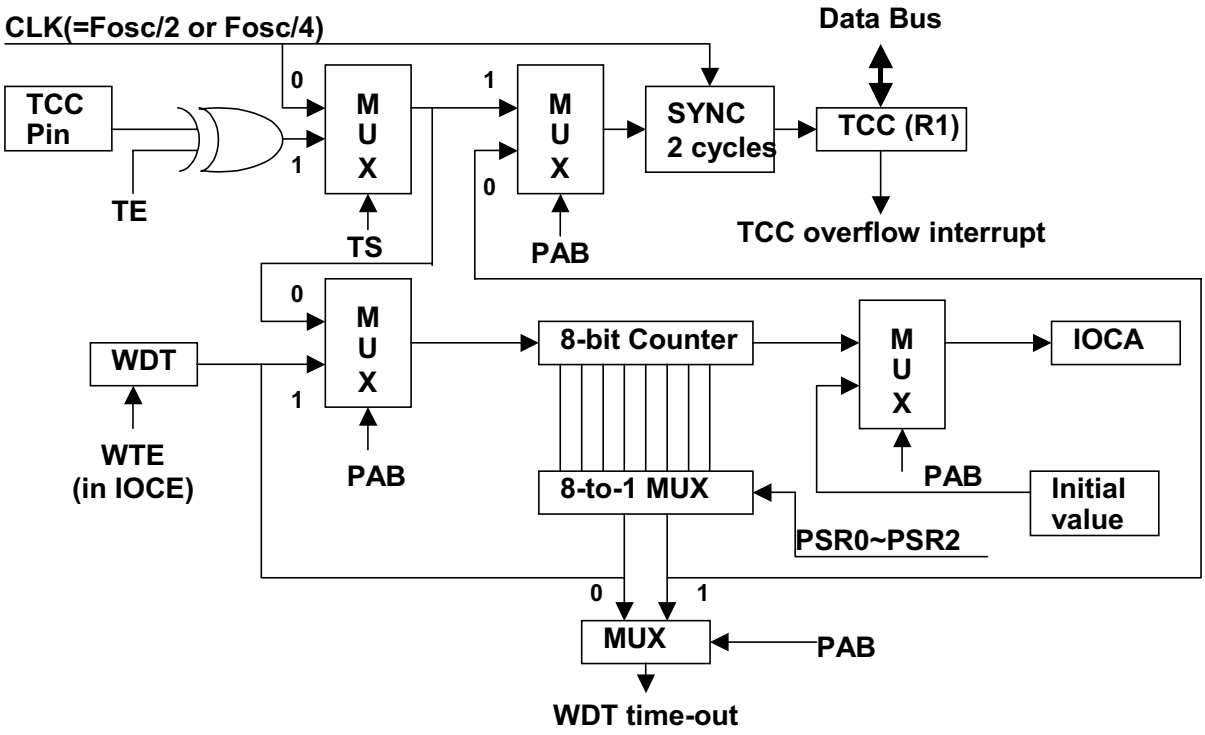
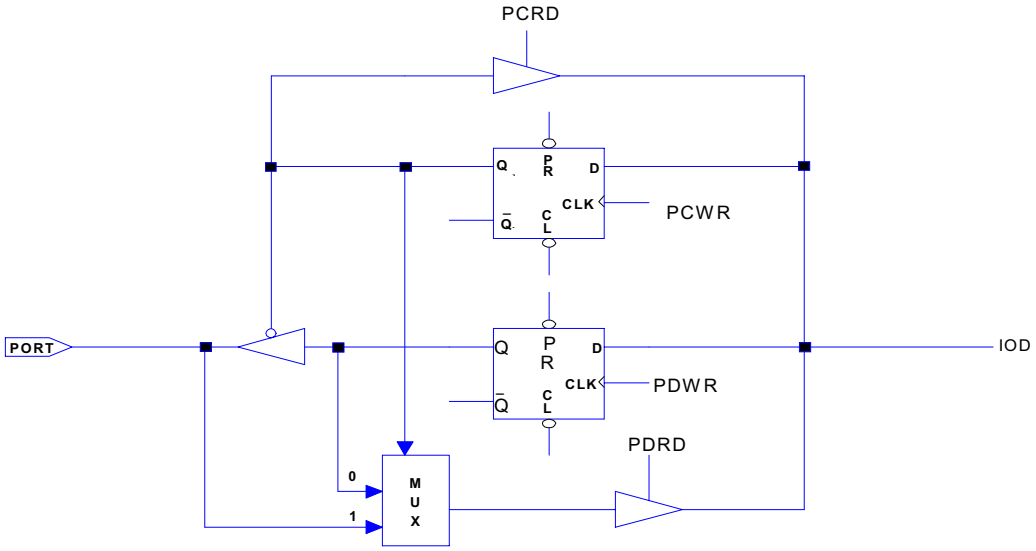


Fig. 5 Block Diagram of TCC and WDT

4.4 I/O Ports

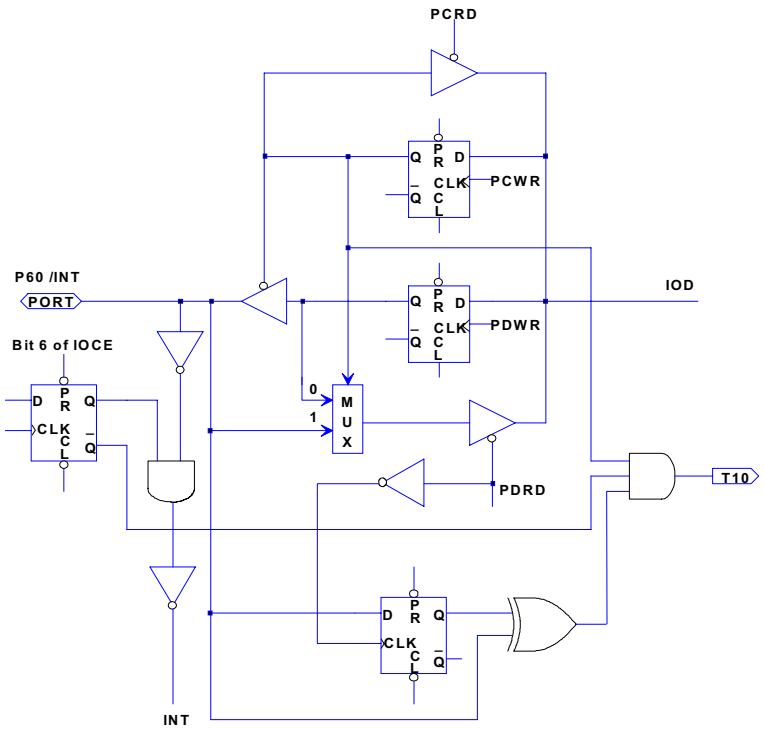
The I/O registers, both Port 5 and Port 6, are bi-directional tri-state I/O ports. Port 6 can be pulled high internally by software. In addition, Port 6 can also have open-drain output by software. Input status change interrupt (or wake-up) function on Port 6. P50 ~ P52 and P60 ~ P63 pins can be pulled down by software. Each I/O pin can be defined as "input" or "output" pin by the I/O control register (IOC5 ~ IOC6). P50~P51 are the R-option pins enabled by setting the ROC bit in the IOCE register to 1. When the R-option function is used, it is recommended that P50~P51 are used as output pins. When R-option is in enable state, P50~P51 must be programmed as input pins. Under R-option mode, the current/power consumption by Rex should be taken into the consideration to promote energy conservation.

The I/O registers and I/O control registers are both readable and writable. The I/O interface circuits for Port 5 and Port 6 are shown in the following Figures 6, 7(a), 7(b), and Figure 8.



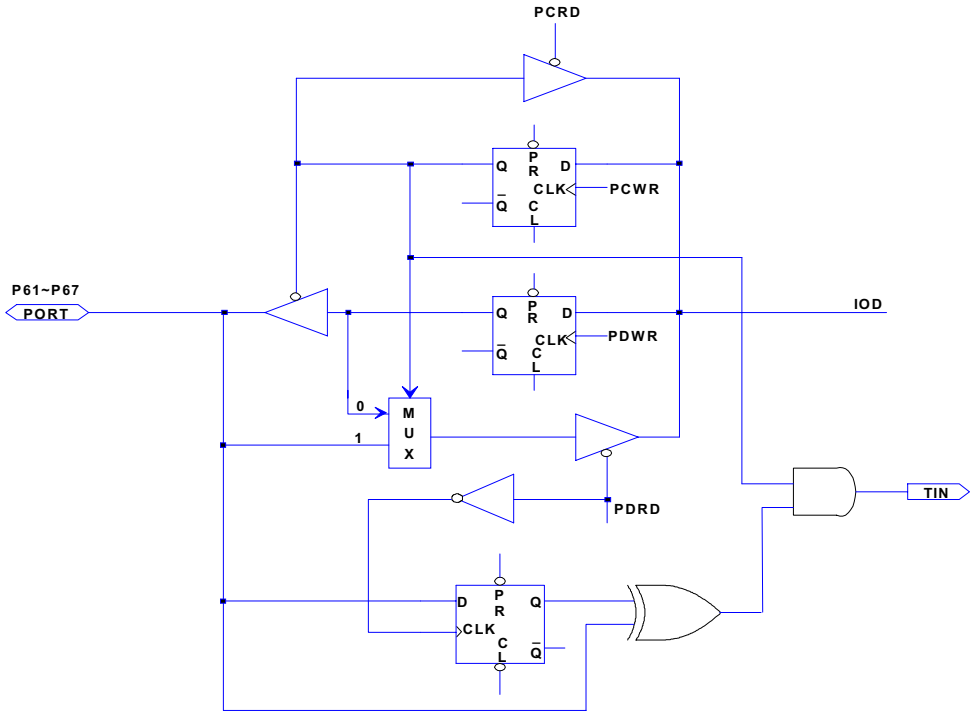
NOTE: Pull-down is not shown in the figure.

Fig. 6 The Circuit of I/O Port and I/O Control Register for Port 5



NOTE: Pull-high (down) and Open-drain are not shown in the figure.

Fig. 7(a) The Circuit of I/O Port and I/O Control Register for P60(/INT)



NOTE: Pull-high (down) and Open-drain are not shown in the figure.

Fig. 7(b) The Circuit of I/O Port and I/O Control Register for P61~P67

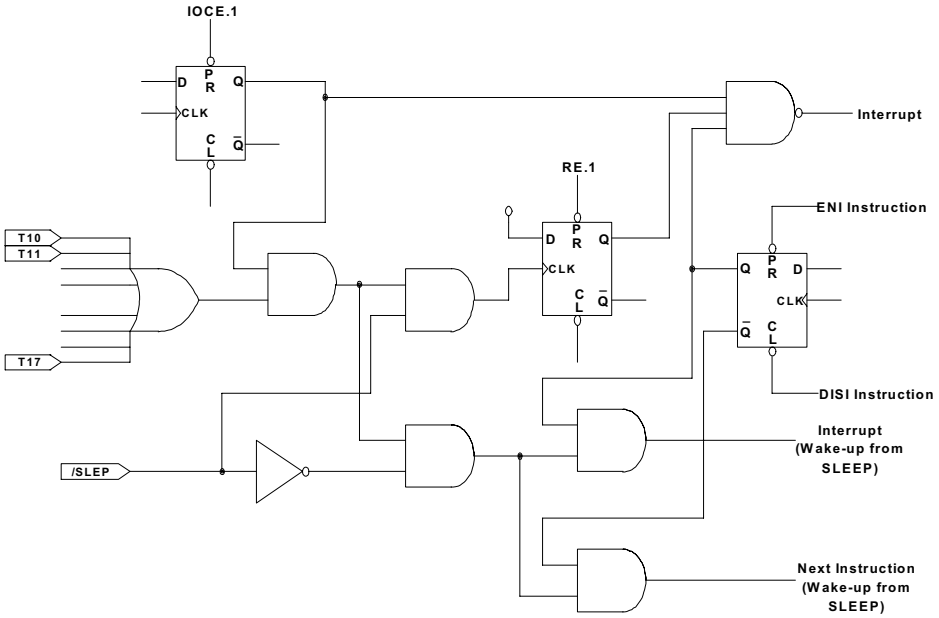
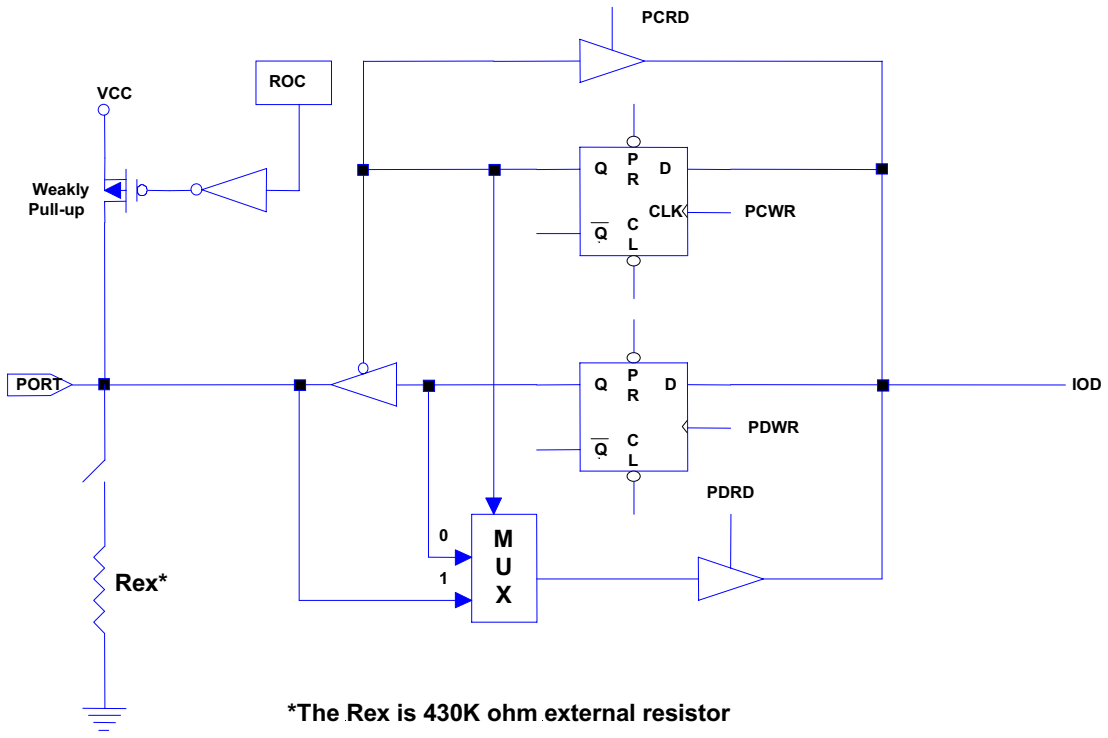


Fig. 7(c) Block Diagram of I/O Port 6 with Input Change Interrupt/Wake-up

Table 4 Usage of Port 6 Input Change Wake-up/Interrupt Function

Usage of Port 6 input status changed Wake-up/Interrupt	
(I) Wake-up from Port 6 Input Status change (a) Before SLEEP 1. Disable WDT[1] (using very carefully) 2. Read I/O Port 6 (MOV R6,R6) 3. Execute "ENI" or "DISI" 4. Enable interrupt (Set IOCF.1) 5. Execute "SLEP" instruction (b) After Wake-up 1. IF "ENI" → Interrupt vector (008H) 2. IF "DISI" → Next instruction	**(II)** Port 6 Input Status Change Interrupt 1. Read I/O Port 6 (MOV R6,R6) 2. Execute "ENI" 3. Enable interrupt (Set IOCF.1) 4. IF Port 6 change (interrupt) → Interrupt vector (008H)



***The Rex is 430K ohm external resistor**

Fig. 8 The Circuit of I/O Port with R-option(P50,P51)

[1] NOTE: Software disables WDT (watchdog timer) but hardware must be enabled before applying Port 6 Changed Wake-up function. (CODE Option Register and Bit 11 (ENWDT) are set to "1").

4.5 RESET and Wake-up

1. RESET

A RESET is initiated by one of the following events-

(1) Power on reset.

(2) /RESET pin input "low",or

(3) WDT time-out (if enabled).

The device is kept in a RESET condition for a period of approx. 18[1]ms (one oscillator start-up timer period) after the reset is detected. Once the RESET occurs, the following functions are performed. Refer to Fig.9.

- The oscillator is running, or will be started.
- The Program Counter (R2) is set to all "0".
- All I/O port pins are configured as input mode (high-impedance state).
- The Watchdog timer and prescaler are cleared.
- When power is switched on, the upper 3 bits of R3 are cleared.
- The bits of the CONT register are set to all "1" except for the Bit 6 (INT flag).
- The bits of the IOCA register are set to all "1".
- The bits of the IOCB register are set to all "1".
- The IOCC register is cleared.
- The bits of the IOCD register are set to all "1".
- Bit 7 of the IOCE register is set to "1", and Bits 4 and 6 are cleared.
- Bits 0~2 of RF and bits 0~2 of IOCF register are cleared.

The sleep (power down) mode is asserted by executing the “SLEP” instruction. While entering sleep mode, WDT (if enabled) is cleared but keeps on running. The controller can be awakened by-

(1) External reset input on /RESET pin,

(2) WDT time-out (if enabled), or

(3) Port 6 input status changes (if enabled).

The first two cases will cause the EM78156E to reset. The T and P flags of R3 can be used to determine the source of the reset (wake-up). The last case is considered the continuation of program execution and the global interrupt ("ENI" or "DISI" being executed) decides whether or not the

[1] NOTE: Vdd = 5V, set up time period = 16.8ms ± 5%
Vdd = 3V, set up time period = 18.6ms ± 5%

controller branches to the interrupt vector following wake-up. If ENI is executed before SLEP, the operation will restart from the succeeding instruction right next to SLEP after wake-up.

Only one of Cases 2 and 3 can be enabled before entering the sleep mode. That is,

[a] if Port 6 Input Status Change Interrupt is enabled before SLEP , WDT must be disabled. by software. However, the WDT bit in the option register remains enabled. Hence, the EM78P156E can be awakened only by Case 1 or 3.

[b] if WDT is enabled before SLEP, Port 6 Input Status Change Interrupt must be disabled. Hence, the EM78P156E can be awakened only by Case 1 or 2. Refer to the section on Interrupt.

If Port 6 Input Status Change Interrupt is used to wake-up the EM78P156E (Case [a] above), the following instructions must be executed before SLEP:

```
MOV A, @xx000110b       ; Select internal TCC clock
CONTW
CLR R1                  ; Clear TCC and prescaler
MOV A, @xxxx1110b       ; Select WDT prescaler
CONTW
WDTC                    ; Clear WDT and prescaler
MOV A, @0xxxxxxxb       ; Disable WDT
IOW RE
MOV R6, R6              ; Read Port 6
MOV A, @00000x1xb       ; Enable Port 6 input change interrupt
IOW RF
ENI (or DISI)           ; Enable (or disable) global interrupt
SLEP                    ; Sleep
NOP
```

One problem user should be aware of, is that after waking up from the sleep mode, WDT would enable automatically. The WDT operation (being enabled or disabled) should be handled appropriately by software after waking up from the sleep mode.

Table 5 The Summary of the Initialized Values for Registers

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	IOC5	Bit Name	X	X	X	X	C53	C52	C51	C50
		Power-On	U	U	U	U	1	1	1	1
		/RESET and WDT	U	U	U	U	1	1	1	1
		Wake-Up from Pin Change	U	U	U	U	P	P	P	P
N/A	IOC6	Bit Name	C67	C66	C65	C64	C63	C62	C61	C60
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
N/A	CONT	Bit Name	X	/INT	TS	TE	PAB	PSR2	PSR1	PSR0
		Power-On	1	0	1	1	1	1	1	1
		/RESET and WDT	1	0	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x00	R0(IAR)	Bit Name	-	-	-	-	-	-	-	-
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x01	R1(TCC)	Bit Name	-	-	-	-	-	-	-	-
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x02	R2(PC)	Bit Name	-	-	-	-	-	-	-	-
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	**0/P	**0/P	**0/P	**0/P	**1/P	**0/P	**0/P	**0/P
0x03	R3(SR)	Bit Name	GP2	GP1	GP0	T	P	Z	DC	C
		Power-On	0	0	0	1	1	U	U	U
		/RESET and WDT	0	0	0	T	t	P	P	P
		Wake-Up from Pin Change	P	P	P	T	t	P	P	P
0x04	R4(RSR)	Bit Name	-	-	-	-	-	-	-	-
		Power-On	1	1	U	U	U	U	U	U
		/RESET and WDT	1	1	P	P	P	P	P	P
		Wake-Up from Pin Change	1	1	P	P	P	P	P	P
0x05	P5	Bit Name	X	X	X	X	P53	P52	P51	P50
		Power-On	0	0	0	0	U	U	U	U
		/RESET and WDT	0	0	0	0	P	P	P	P
		Wake-Up from Pin Change	0	0	0	0	P	P	P	P
0x06	P6	Bit Name	P67	P66	P65	P64	P63	P62	P61	P60
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x0F	RF(ISR)	Bit Name	X	X	X	X	X	EXIF	ICIF	TCIF
		Power-On	U	U	U	U	U	0	0	0
		/RESET and WDT	U	U	U	U	U	0	0	0
		Wake-Up from Pin Change	U	U	U	U	U	P	P	P
0x0A	IOCA	Bit Name	-	-	-	-	-	-	-	-
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x0B	IOCB	Bit Name	/PD7	/PD6	/PD5	/PD4	X	/PD2	/PD1	/PD0
		Power-On	1	1	1	1	U	1	1	1
		/RESET and WDT	1	1	1	1	U	1	1	1
		Wake-Up from Pin Change	P	P	P	P	U	P	P	P
0x0C	IOCC	Bit Name	OD7	OD6	OD5	OD4	OD3	OD2	OD1	OD0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x0D	IOCD	Bit Name	/PH7	/PH6	/PH5	/PH4	/PH3	/PH2	/PH1	/PH0
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x0E	IOCE	Bit Name	WDTE	EIS	X	ROC	X	X	X	X
		Power-On	1	0	U	0	U	U	U	U
		/RESET and WDT	1	0	U	0	U	U	U	U
		Wake-Up from Pin Change	1	P	U	P	U	U	U	U
0x0F	IOCF	Bit Name	X	X	X	X	X	EXIE	ICIE	TCIE
		Power-On	U	U	U	U	U	0	0	0
		/RESET and WDT	U	U	U	U	U	0	0	0
		Wake-Up from Pin Change	U	U	U	U	U	P	P	P
0x10~0x2F	R10~R2F	Bit Name	-	-	-	-	-	-	-	-
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P

** To jump address 0x08, or to execute the instruction which is next to the “SLEP” instruction.

X: Not used. U: Unknown or don’t care. P: Previous value before reset. t: Check Table 6

2. The Status of RST, T, and P of STATUS Register

A RESET condition is initiated by the following events:

1. A power-on condition,
2. A high-low-high pulse on /RESET pin, and

3. Watchdog timer time-out.

The values of T and P, listed in Table 6 are used to check how the processor wakes up. Table 7 shows the events that may affect the status of T and P.

Table 6 The Values of RST, T and P after RESET

Reset Type	T	P
Power on	1	1
/RESET during Operating mode	*P	*P
/RESET wake-up during SLEEP mode	1	0
WDT during Operating mode	0	*P
WDT wake-up during SLEEP mode	0	0
Wake-Up on pin change during SLEEP mode	1	0

*P: Previous status before reset

Table 7 The Status of T and P Being Affected by Events.

Event	T	P
Power on	1	1
WDTC instruction	1	1
WDT time-out	0	*P
SLEP instruction	1	0
Wake-Up on pin change during SLEEP mode	1	0

*P: Previous value before reset

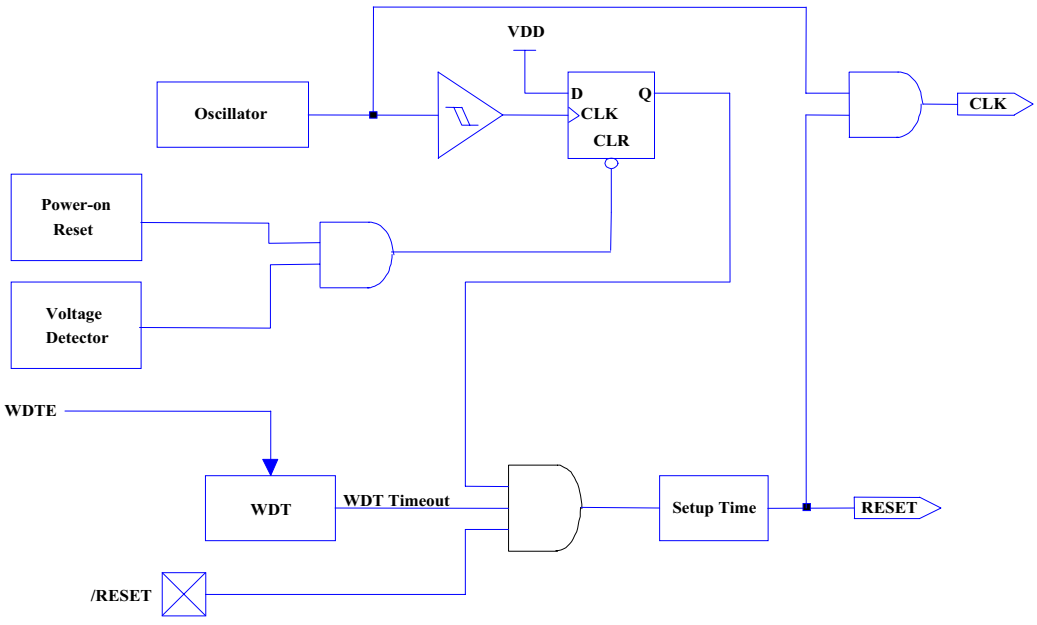


Fig. 9 Block Diagram of Controller Reset

4.6 Interrupt

The EM78156E has three falling-edge interrupts listed below:

(1) TCC overflow interrupt

(2) Port 6 Input Status Change Interrupt

(3) External interrupt [(P60, /INT) pin].

Before the Port 6 Input Status Change Interrupt is enabled, reading Port 6 (e.g. "MOV R6,R6") is necessary. Each pin of Port 6 will have this feature if its status changed. Any pin configured as output or P60 pin configured as /INT is excluded from this function. The Port 6 Input Status Changed Interrupt can wake up the EM78P156EL from the sleep mode if Port 6 is enabled prior to going into the sleep mode by executing SLEP. When the chip wakes-up, the controller will continue to execute the succeeding address if the global interrupt is disabled or branch to the interrupt vector 008H if the global interrupt is enabled.

RF is the interrupt status register that records the interrupt requests in the relative flags/bits. IOCF is an interrupt mask register. The global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. When one of the interrupts (enabled) occurs, the next instruction will be fetched from address 008H. Once in the interrupt service routine, the source of an interrupt can be determined by polling the flag bits in RF. The interrupt flag bit must be cleared by instructions before leaving the interrupt service routine and before interrupts are enabled to avoid recursive interrupts.

The flag (except ICIF bit) in the Interrupt Status Register (RF) is set regardless of the status of its mask bit or the execution of ENI. Note that the outcome of RF will be the logic AND of RF and IOCF (refer to Fig. 10). The RETI instruction ends the interrupt routine and enables the global interrupt (the execution of ENI).

When an interrupt is generated by the INT instruction (enabled), the next instruction will be fetched from address 001H.

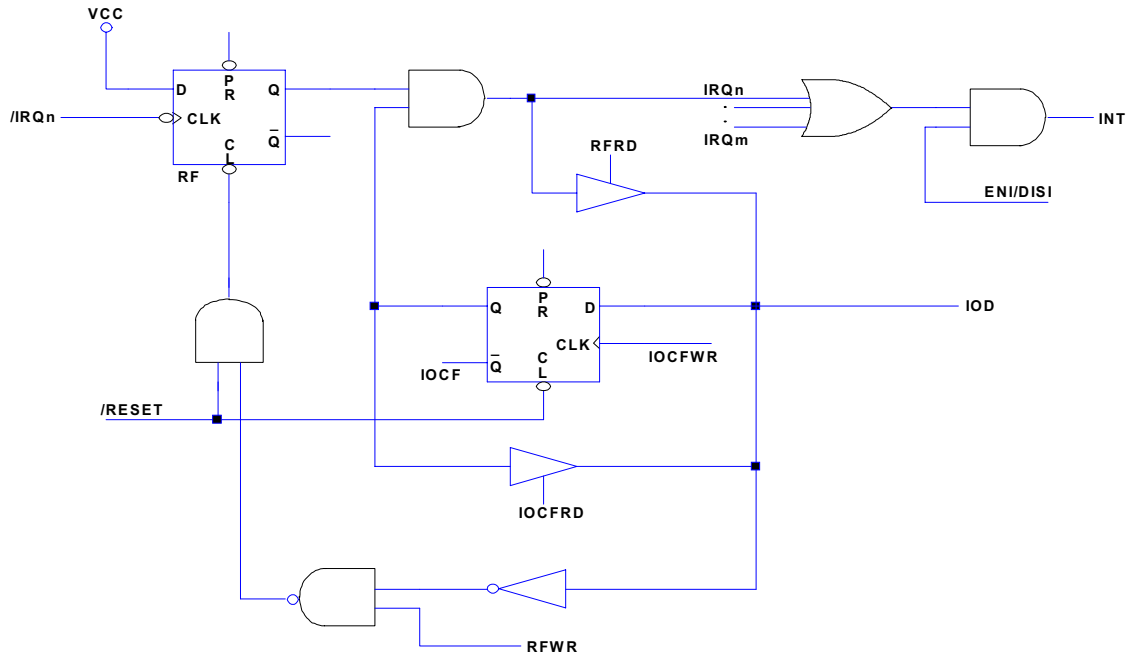


Fig. 10 Interrupt Input Circuit

4.7 Oscillator

1. Oscillator Modes

The EM78156E can be operated in three different oscillator modes, such as External RC oscillator mode (ERC), High XTAL oscillator mode(HXT), and Low XTAL oscillator mode(LXT). User can select one of them by programming MS and HLF in the CODE option register. Table 8 depicts how these three modes are defined.

The up-most limited operation frequency of crystal/resonator on the different VDDs is listed in Table 9.

Table 8 Oscillator Modes Defined by MS and HLP

Mode	MS	HLF
ERC(External RC oscillator mode)	0	*X
HXT(High XTAL oscillator mode)	1	1
LXT(Low XTAL oscillator mode)	1	0

<Note> 1. X, Don't care

2. The transient point of system frequency between HXT and LXY is around 400 KHz.

Table 9 The Summary of Maximum Operating Speeds

Conditions	VDD	Fxt max.(MHz)
Two cycles with two clocks	2.3	4.0
	3.0	8.0
	5.0	20.0

2 .Crystal Oscillator/Ceramic Resonators(XTAL)

EM78156E can be driven by an external clock signal through the OSCI pin as shown in Fig. 11 below.

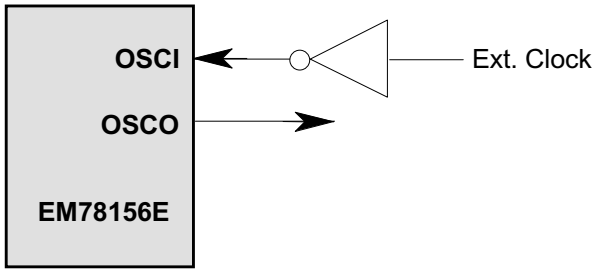


Fig. 11 Circuit for External Clock Input

In the most applications, Pin OSCI and Pin OSCO can be connected with a crystal or ceramic resonator to generate oscillation. Fig. 12 depicts such circuit. The same thing applies whether it is in the HXT mode or in the LXT mode. Table 10 provides the recommended values of C1 and C2. Since each resonator has its own attribute, user should refer to its specification for appropriate values of C1 and C2. RS, a serial resistor, may be necessary for AT strip cut crystal or low frequency mode.

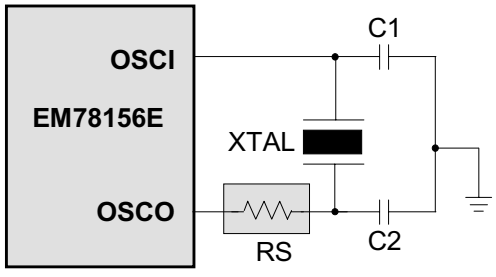


Fig. 12 Circuit for Crystal/Resonator

Table 10 Capacitor Selection Guide for Crystal Oscillator or Ceramic Resonator

Oscillator Type	Frequency Mode	Frequency	C1(pF)	C2(pF)
Ceramic Resonators	HXT	455 kHz	100~150	100~150
		2.0 MHz	20~40	20~40
		4.0 MHz	10~30	10~30
Crystal Oscillator	LXT	32.768kHz	25	15
		100KHz	25	25
		200KHz	25	25
	HXT	455KHz	20~40	20~150
		1.0MHz	15~30	15~30
		2.0MHz	15	15
		4.0MHz	15	15

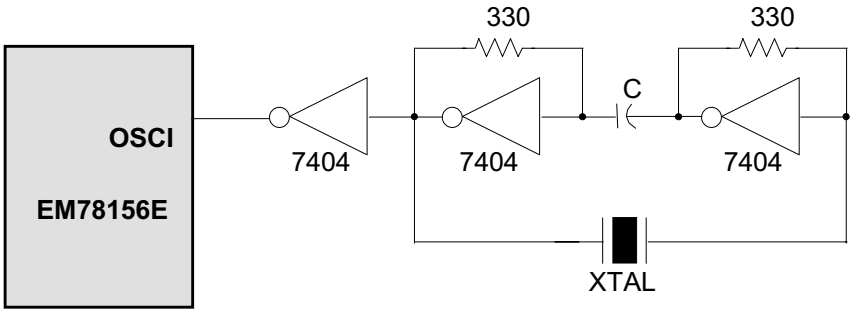


Fig. 13 Circuit for Crystal/Resonator-Series Mode

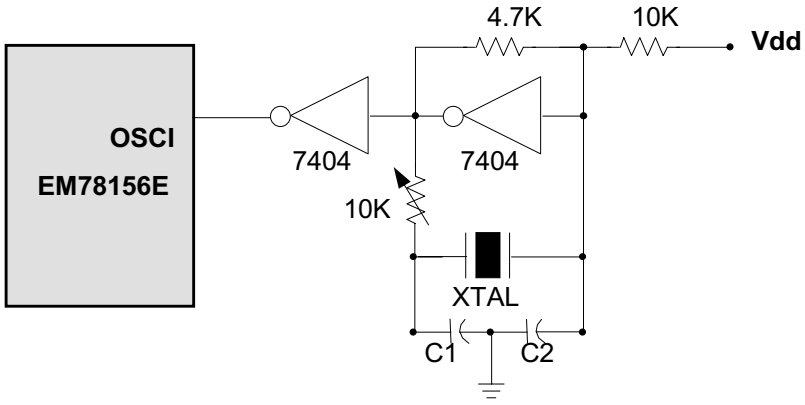


Fig. 14 Circuit for Crystal/Resonator-Parallel Mode

3. External RC Oscillator Mode

For some applications that do not need a very precise timing calculation, the RC oscillator (Fig. 15) offers a lot of cost savings. Nevertheless, it should be noted that the frequency of the RC oscillator is influenced by the supply voltage, the values of the resistor (Rext), the capacitor (Cext), and even by the operation temperature. Moreover, the frequency also changes slightly from one chip to another due to the manufacturing process variation.

In order to maintain a stable system frequency, the values of the Cext should not be less than 20pF, and that the value of Rext should not be greater than 1 M ohm. If they cannot be kept in this range, the frequency is easily affected by noise, humidity, and leakage.

The smaller the Rext in the RC oscillator, the faster its frequency will be. On the contrary, for very low Rext values, for instance, 1 KΩ, the oscillator becomes unstable because the NMOS cannot discharge the current of the capacitance correctly.

Based on the above reasons, it must be kept in mind that all of the supply voltage, the operation temperature, the components of the RC oscillator, the package types, the way the PCB is layout, will affect the system frequency.

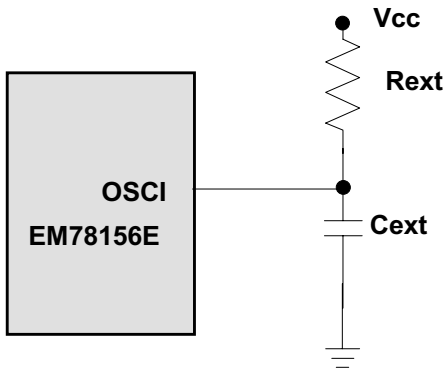


Fig. 15 Circuit for External RC Oscillator Mode

Table 11 RC Oscillator Frequencies

Cext	Rext	Average Fosc 5V,25°C	Average Fosc 3V,25°C
20 pF	3.3k	3.92 MHz	3.65 MHz
	5.1k	2.67 MHz	2.60 MHz
	10k	1.39 MHz	1.40 MHz
	100k	149 KHz	156 KHz

100 pF	3.3k	1.39 MHz	1.33 MHz
	5.1k	940 KHz	920 KHz
	10k	480 KHz	475 KHz
	100k	52 KHz	50 KHz
300 pF	3.3k	595 KHz	560 KHz
	5.1k	400 KHz	390 KHz
	10k	200 KHz	200 KHz
	100k	21 KHz	20 KHz

<Note> 1. Measured on DIP packages.

2. For design reference only.

4.8 CODE Option Register

The EM78P156E has a CODE option word that is not a part of the normal program memory. The option bits cannot be accessed during normal program execution.

Bit0	Bit1	Bit2	Bit3	Bit4	Bit5
LVDD	CLK	/ENWDT	HLF	MS	-

• **Bit 0 (LVDD)**: Levels of the Operating Voltage.

0: Operating Voltage 2.3V ~ 5.5V, non-power saving.

1: Operating Voltage 4V ~ 5.5V, power saving.

• **Bit 1 (CLK)**: Instruction period option bit.

0: two oscillator periods.

1: four oscillator periods.

Refer to the section on Instruction Set.

• **Bit 2 (/ENWDT)**: Watchdog timer enable bit.

0: Enable

1: Disable

• **Bit 3 (HLF)**: XTAL frequency selection

0: XTAL2 type (low frequency, 32.768KHz)

1: XTAL1 type (high frequency)

This bit will affect system oscillation only when Bit4(MS) is “1”. When MS is”0”, HLF must be “0”.

<Note>: The transient point of system frequency between HXT and LXY is around 400 KHz.

• **Bit 4 (MS)**:Oscillator type selection.

0: RC type

1: XTAL type (XTAL1 and XTAL2)

• **Bit 5**: Reserved.

The bit is set to “1” all the time.

4.9 Power On Considerations

Any microcontroller is not guaranteed to start to operate properly before the power supply stays at its steady state. EM78P156E is equipped with Power On Voltage Detector (POVD) with a detecting level of 1.8V. It will work well if Vdd rise quick enough (50 ms or less). In many critical applications, however, extra devices are still required to assist in solving power-up problems.

4.10 External Power On Reset Circuit

The circuit shown in Fig.16 implements an external RC to produce the reset pulse. The pulse width (time constant) should be kept long enough for Vdd to reached minimum operation voltage. This circuit is used when the power supply has slow rise time. Because the current leakage from the /RESET pin is about ±5μA, it is recommended that R should not be greater than 40 K. In this way, the /RESET pin voltage is held below 0.2V. The diode (D) acts as a short circuit at the moment of power down. The capacitor C will discharge rapidly and fully. Rin, the current-limited resistor, will prevent high current or ESD (electrostatic discharge) from flowing to pin /RESET.

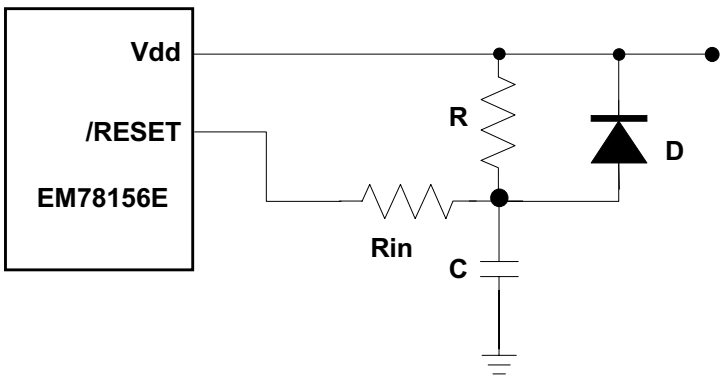


Fig. 16 External Power-Up Reset Circuit

4.11 Residue-Voltage Protection

When battery is replaced, device power (Vdd) is taken off but residue-voltage remains. The residue-voltage may trips below Vdd minimum, but not to zero. This condition may cause a poor power on reset. Fig.17 and Fig.18 show how to build a residue-voltage protection circuit.

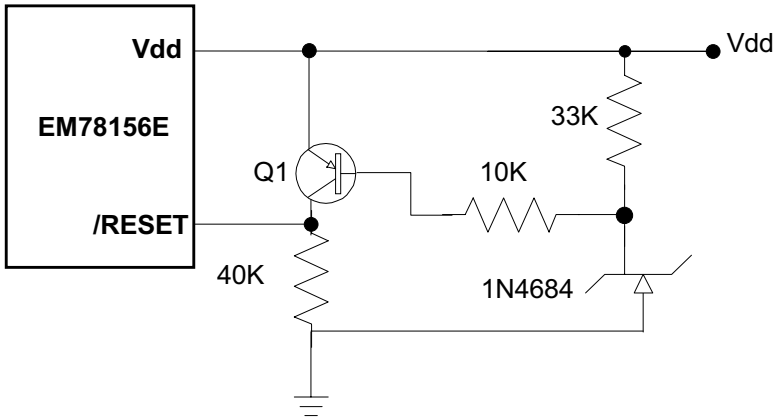


Fig. 17 Circuit 1 for the Residue Voltage Protection

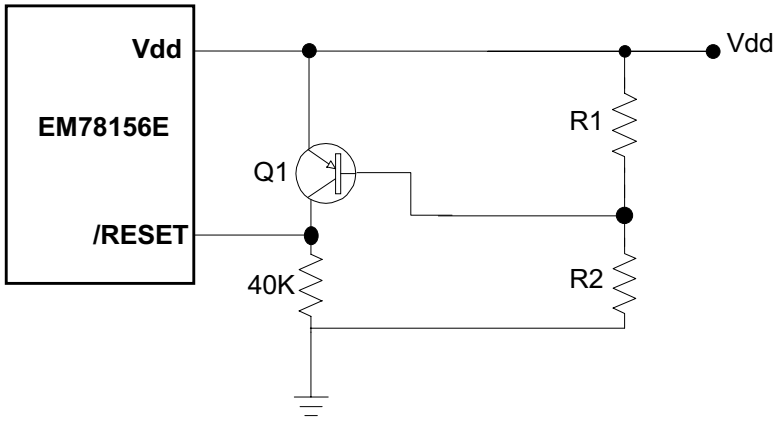


Fig. 18 Circuit 2 for the Residue Voltage Protection

4.12 Instruction Set

Each instruction in the instruction set is a 13-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of 2 oscillator periods), unless the program counter is changed by instruction "MOV R2,A", "ADD R2,A", or by instructions of arithmetic or logic operation on R2 (e.g. "SUB R2,A", "BS(C) R2,6", "CLR R2", ····). In this case, the execution takes two instruction cycles.

If for some reasons, the specification of the instruction cycle is not suitable for certain applications, try modifying the instruction as follows:

(A) Change one instruction cycle to consist of 4 oscillator periods.

(B) "JMP", "CALL", "RET", "RETL", "RETI", or the conditional skip ("JBS", "JBC", "JZ", "JZA", "DJZ", "DJZA") commands which were tested to be true, are executed within two instruction cycles. The instructions that are written to the program counter also take two instruction cycles.

Case (A) is selected by the CODE Option bit, called CLK. One instruction cycle consists of two oscillator clocks if CLK is low, and four oscillator clocks if CLK is high.

Note that once the 4 oscillator periods within one instruction cycle is selected as in Case (A), the internal clock source to TCC should be CLK=Fosc/4, not Fosc/ 2 as shown in Fig. 5.

In addition, the instruction set has the following features:

(1) Every bit of any register can be set, cleared, or tested directly.

(2) The I/O register can be regarded as general register. That is, the same instruction can operate on I/O register.

The symbol "R" represents a register designator that specifies which one of the registers (including operational registers and general purpose registers) is to be utilized by the instruction. "b" represents a bit field designator that selects the value for the bit which is located in the register "R", and affects operation. "k" represents an 8 or 10-bit constant or literal value.

INSTRUCTION BINARY	HEX	MNEMONIC	OPERATION	STATUS AFFECTED
0 0000 0000 0000	0000	NOP	No Operation	None
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C
0 0000 0000 0010	0002	CONTW	A → CONT	None
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T,P
0 0000 0000 0100	0004	WDTC	0 → WDT	T,P
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None <Note1>
0 0000 0001 0000	0010	ENI	Enable Interrupt	None
0 0000 0001 0001	0011	DISI	Disable Interrupt	None
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC, Enable Interrupt	None
0 0000 0001 0100	0014	CONTR	CONT → A	None
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None <Note1>
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None
0 0000 1000 0000	0080	CLRA	0 → A	Z
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z
0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z,C,DC
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z,C,DC
0 0001 10rr rrrr	01rr	DECA R	R-1 → A	Z
0 0001 11rr rrrr	01rr	DEC R	R-1 → R	Z
0 0010 00rr rrrr	02rr	OR A,R	A ∨ R → A	Z
0 0010 01rr rrrr	02rr	OR R,A	A ∨ R → R	Z
0 0010 10rr rrrr	02rr	AND A,R	A & R → A	Z

0 0010 11rr rrrr	02rr	AND R,A	A & R → R	Z
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R → A	Z
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R → R	Z
0 0011 10rr rrrr	03rr	ADD A,R	A + R → A	Z,C,DC
0 0011 11rr rrrr	03rr	ADD R,A	A + R → R	Z,C,DC
0 0100 00rr rrrr	04rr	MOV A,R	R → A	Z
0 0100 01rr rrrr	04rr	MOV R,R	R → R	Z
0 0100 10rr rrrr	04rr	COMA R	/R → A	Z
0 0100 11rr rrrr	04rr	COM R	/R → R	Z
0 0101 00rr rrrr	05rr	INCA R	R+1 → A	Z
0 0101 01rr rrrr	05rr	INC R	R+1 → R	Z
0 0101 10rr rrrr	05rr	DJZA R	R-1 → A, skip if zero	None
0 0101 11rr rrrr	05rr	DJZ R	R-1 → R, skip if zero	None
0 0110 00rr rrrr	06rr	RRCA R	R(n) → A(n-1), R(0) → C, C → A(7)	C
0 0110 01rr rrrr	06rr	RRC R	R(n) → R(n-1), R(0) → C, C → R(7)	C
0 0110 10rr rrrr	06rr	RLCA R	R(n) → A(n+1), R(7) → C, C → A(0)	C
0 0110 11rr rrrr	06rr	RLC R	R(n) → R(n+1), R(7) → C, C → R(0)	C
0 0111 00rr rrrr	07rr	SWAPA R	R(0-3) → A(4-7), R(4-7) → A(0-3)	None
0 0111 01rr rrrr	07rr	SWAP R	R(0-3) ↔ R(4-7)	None
0 0111 10rr rrrr	07rr	JZA R	R+1 → A, skip if zero	None
0 0111 11rr rrrr	07rr	JZ R	R+1 → R, skip if zero	None
0 100b bbrr rrrr	0xxx	BC R,b	0 → R(b)	None <Note2>
0 101b bbrr rrrr	0xxx	BS R,b	1 → R(b)	None <Note3>
0 110b bbrr rrrr	0xxx	JBC R,b	if R(b)=0, skip	None
0 111b bbrr rrrr	0xxx	JBS R,b	if R(b)=1, skip	None
1 00kk kkkk kkkk	1kkk	CALL k	PC+1 → [SP], (Page, k) → PC	None
1 01kk kkkk kkkk	1kkk	JMP k	(Page, k) → PC	None
1 1000 kkkk kkkk	18kk	MOV A,k	k → A	None
1 1001 kkkk kkkk	19kk	OR A,k	A ∨ k → A	Z
1 1010 kkkk kkkk	1Akk	AND A,k	A & k → A	Z
1 1011 kkkk kkkk	1Bkk	XOR A,k	A ⊕ k → A	Z
1 1100 kkkk kkkk	1Ckk	RETL k	k → A, [Top of Stack] → PC	None
1 1101 kkkk kkkk	1Dkk	SUB A,k	k-A → A	Z,C,DC
1 1110 0000 0001	1E01	INT	PC+1 → [SP], 001H → PC	None
1 1111 kkkk kkkk	1Fkk	ADD A,k	k+A → A	Z,C,DC

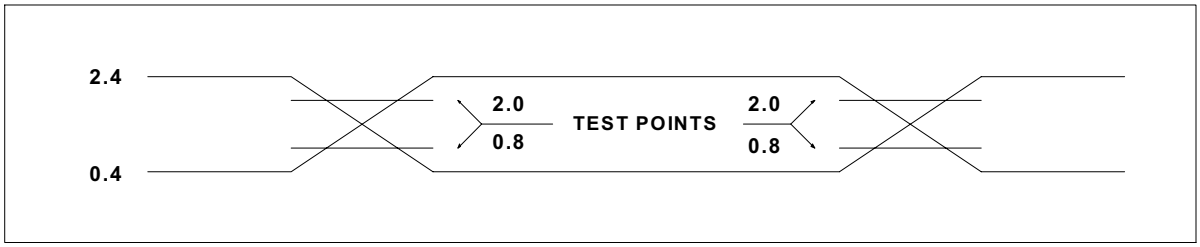
<Note 1> This instruction is applicable to IOC5~IOC6, IOCB~IOCF only.

<Note 2> This instruction is not recommended for RF operation.

<Note 3> This instruction cannot operate under RF.

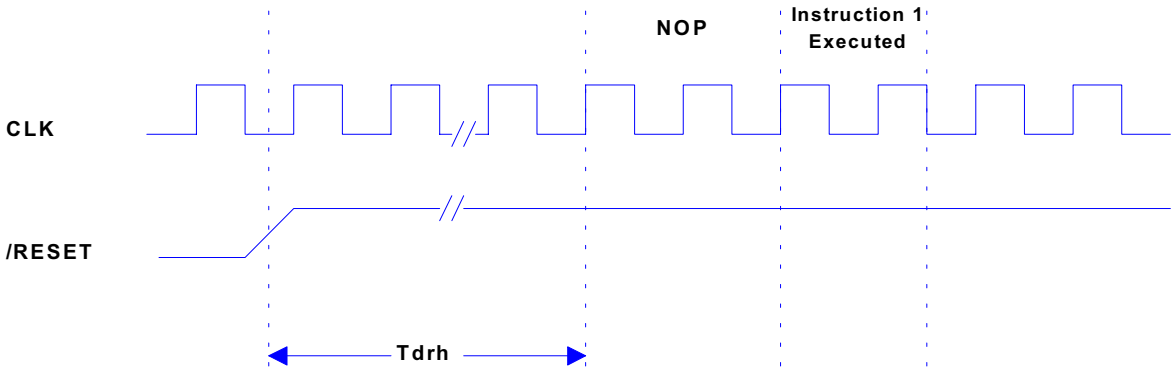
4.13 Timing Diagrams

AC Test Input/Output Waveform

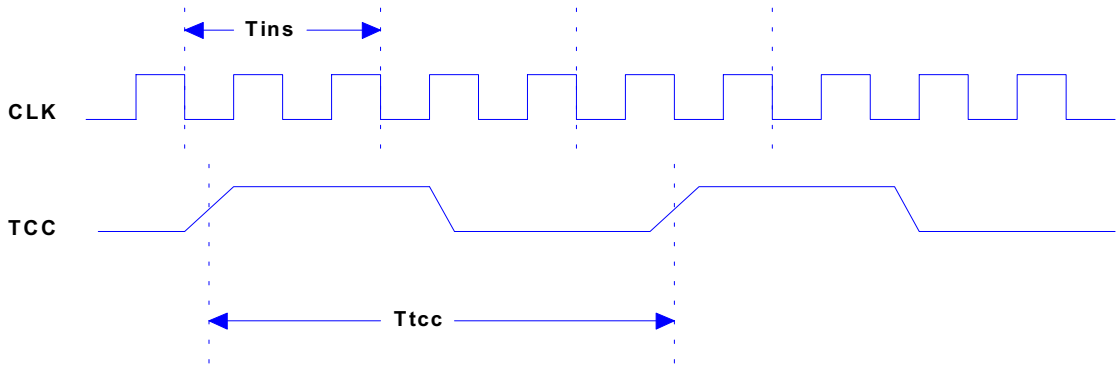


AC Testing : Input is driven at 2.4V for logic "1",and 0.4V for logic "0".Timing measurements are made at 2.0V for logic "1",and 0.8V for logic "0".

RESET Timing (CLK="0")



TCC Input Timing (CLKS="0")



5. ABSOLUTE MAXIMUNM RATINGS

Items	Rating
Temperature under bias	0°C to 70°C
Storage temperature	-65°C to 150°C
Input voltage	-0.3V to +6.0V
Output voltage	-0.3V to +6.0V

6. ELECTRICAL CHARACTERISTICS

6.1 DC Electrical Characteristic

(Ta= 0°C ~ 70 °C, VDD= 5.0V±5%, VSS= 0V)

Symbol	Parameter	Condition	Min	Typ.	Max	Unit
FXT	XTAL: VDD to 3V	Two cycle with two clocks	DC		8.0	MHz
	XTAL: VDD to 5V	Two cycle with two clocks	DC		20.0	MHz
ERC	ERC: VDD to 5V	R: 5.1KΩ, C: 100 pF	F±30%	940	F±30%	KHz
IIL	Input Leakage Current for input pins	VIN = VDD, VSS			±1	μA
VIH1	Input High Voltage (VDD=5V)	Ports 5, 6	2.0			V
VIL1	Input Low Voltage (VDD=5V)	Ports 5, 6			0.8	V
VIHT1	Input High Threshold Voltage (VDD=5V)	/RESET, TCC	2.0			V
VILT1	Input Low Threshold Voltage (VDD=5V)	/RESET, TCC			0.8	V
VIHX1	Clock Input High Voltage (VDD=5V)	OSCI	3.5			V
VILX1	Clock Input Low Voltage (VDD=5V)	OSCI			1.5	V
VIH2	Input High Voltage (VDD=3V)	Ports 5, 6	1.5			V
VIL2	Input Low Voltage (VDD=3V)	Ports 5, 6			0.4	V
VIHT2	Input High Threshold Voltage (VDD=3V)	/RESET, TCC	1.5			V
VILT2	Input Low Threshold Voltage (VDD=3V)	/RESET, TCC			0.4	V
VIHX2	Clock Input High Voltage (VDD=3V)	OSCI	2.1			V
VILX2	Clock Input Low Voltage (VDD=3V)	OSCI			0.9	V
VOH1	Output High Voltage (Ports 5, 6)	IOH = -12.0 mA	2.4			V
VOL1	Output Low Voltage (Ports 5, 6)	IOL = 9.0 mA			0.4	V
IPH	Pull-high current	Pull-high active, input pin at VSS	-50	-70	-240	μA
IPD	Pull-down current	Pull-down active, input pin at VDD	25	50	120	μA
ISB_1	Power down current	All input and I/O pins at VDD, output pin floating, WDT disabled			1	μA
ISB_2	Power down current	All input and I/O pins at VDD, output pin floating, WDT enabled			10	μA
ICC1	Operating supply current (VDD=3V) at two cycles/four clocks	/RESET= 'High', Fosc=32KHz (Crystal type,CLKS="0"), output pin floating, WDT disabled	15	15	30	μA
ICC2	Operating supply current (VDD=3V) at two cycles/four clocks	/RESET= 'High', Fosc=32KHz (Crystal type,CLKS="0"), output pin floating, WDT enabled		20	35	μA
ICC3	Operating supply current (VDD=5.0V) at two cycles/two clocks	/RESET= 'High', Fosc=4MHz (Crystal type, CLKS="0"), output pin floating, WDT enabled			1.6	mA
ICC4	Operating supply current (VDD=5.0V) at two cycles/four clocks	/RESET= 'High', Fosc=10MHz (Crystal type, CLKS="0"), output pin floating, WDT enabled			4.0	mA

6.2 AC Electrical Characteristic

(Ta=0°C ~ 70 °C, VDD=5V±5%, VSS=0V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dclk	Input CLK duty cycle		45	50	55	%
Tins	Instruction cycle time (CLKS="0")	Crystal type	100		DC	ns
		RC type	500		DC	ns
Ttcc	TCC input period		(Tins+20)/N*			ns
Tdrh	Device reset hold time	Ta = 25°C	17.6	16.8	16	ms
Trst	/RESET pulse width	Ta = 25°C	2000			ns
Twdt	Watchdog timer period	Ta = 25°C	17.6	16.8	16	ms
Tset	Input pin setup time			0		ns
Thold	Input pin hold time			20		ns
Tdelay	Output pin delay time	Cload=20pF		50		ns

* N= selected prescaler ratio.

APPENDIX

Package Types:

MASK MCU	Package Type	Pin Count	Package Size
EM78156EP	DIP	18	300 mil
EM78156EM	SOP	18	300 mil
EM78156EAS	SSOP	20	209 mil
EM78156EKM	SSOP	20	209 mil